**Experiment / Assignment / Tutorial No. 02**

**Grade: AA / AB / BB / BC / CC / CD /DD**

**Signature of the Staff In-charge with date**

|  |
| --- |
| Batch: B2 Roll No.: 1611103 Experiment / assignment / tutorial No.: 2 |

|  |
| --- |
| **Title:** Binary Adders and Subtractors |

**\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

**Objective:** To implement half and full adder–subtractor using gates and IC 7483

**\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**\_\_\_\_\_\_\_\_

**Expected Outcome of Experiment:**

**CO2:** Use different minimization technique and solve combinational circuits, synchronous & asynchronous sequential circuits.

**\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

**Books/ Journals/ Websites referred:**

* R. P. Jain, “Modern Digital Electronics”, Tata McGraw Hill
* M .Morris Mano, “Digital Logic & computer Design”, PHI
* http://physics.niser.ac.in/labmanuals/sem5/elect/7\_ADDER%20SUBTRACTO  [R%20CIRCUITS.pd](http://physics.niser.ac.in/labmanuals/sem5/elect/7_ADDER%20SUBTRACTOR%20CIRCUITS.pdf)f

**Pre Lab/ Prior Concepts:**

**Adder:** Addition of two binary digits is most basic operation performed by the digital computer. There are two types of adder:

* Half adder
* Full adder

**Half Adder:** Half adder is combinational logic circuit with two inputs and two outputs. It is the basic building block for addition of two single bit numbers.

**Full adder:** A half adder has a provision not to add a carry coming from the lower order bits when multi bit addition is performed. for this purpose a third input terminal is added and this circuits is to add A,B,C where A and B are the nth order bits of the number A and B respectively and C is the carry generated from the addition of (n-1) order bits. This circuit is referred to as full adder.

**Subtractor:** Subtraction of two binary digits is one of the most basic operations performed by digital computer .there are two types of subtractor:

* Half subtractor
* Full subtractor

**Half subtractor:** Logic circuit for the subtraction of B from A where A,B are 1 bit numbers is referred to as half subtract or .the subtract or process has two input and difference and borrow are the two outputs.

**Full subtractor:** As in the case of the addition using logic gates, a full subtractor is made by combining two half-sub tractors and an additional OR-gate. A full subtractor has the borrow in capability (denoted as BORIN) and so allows cascading which results in the possibility of multi-bit subtraction.

**IC 7483**

For subtraction of one binary number from another, we do so by adding 2’s complement of the former to the latter number using a full adder circuit.

IC 7483 is a 16 pin, 4-bit full adder. This IC has a provision to add the carry output to transfer and end around carry output using Co and C4 respectively.

**2’s complement:** 2’s complement of any binary no. can be obtained by adding 1 in 1’scomplement of that no.

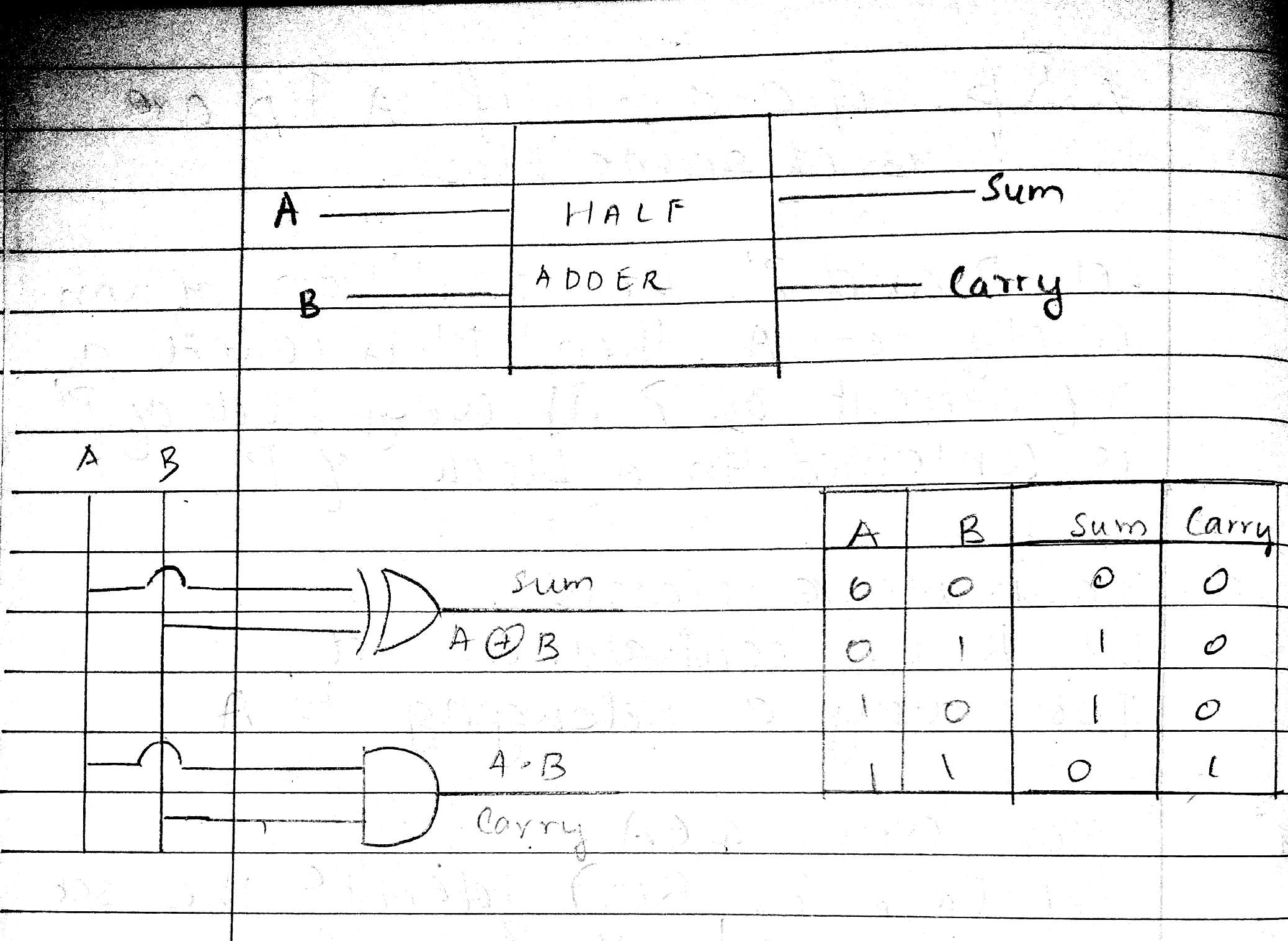
e.g. 2’s complement of +(10)10 =1010is

|  |  |  |  |
| --- | --- | --- | --- |
| 1C of 1010 |  | | 0101 |
|  |  | + | 1 |
| -(10)10 |  | | 0110 |

In 2’s complement subtraction using IC 7483, we are representing negative number in 2’s complement form and then adding it with 1st number.

**Implementation Details:**

**Half Adder Block Diagram Truth Table for Half Adder**

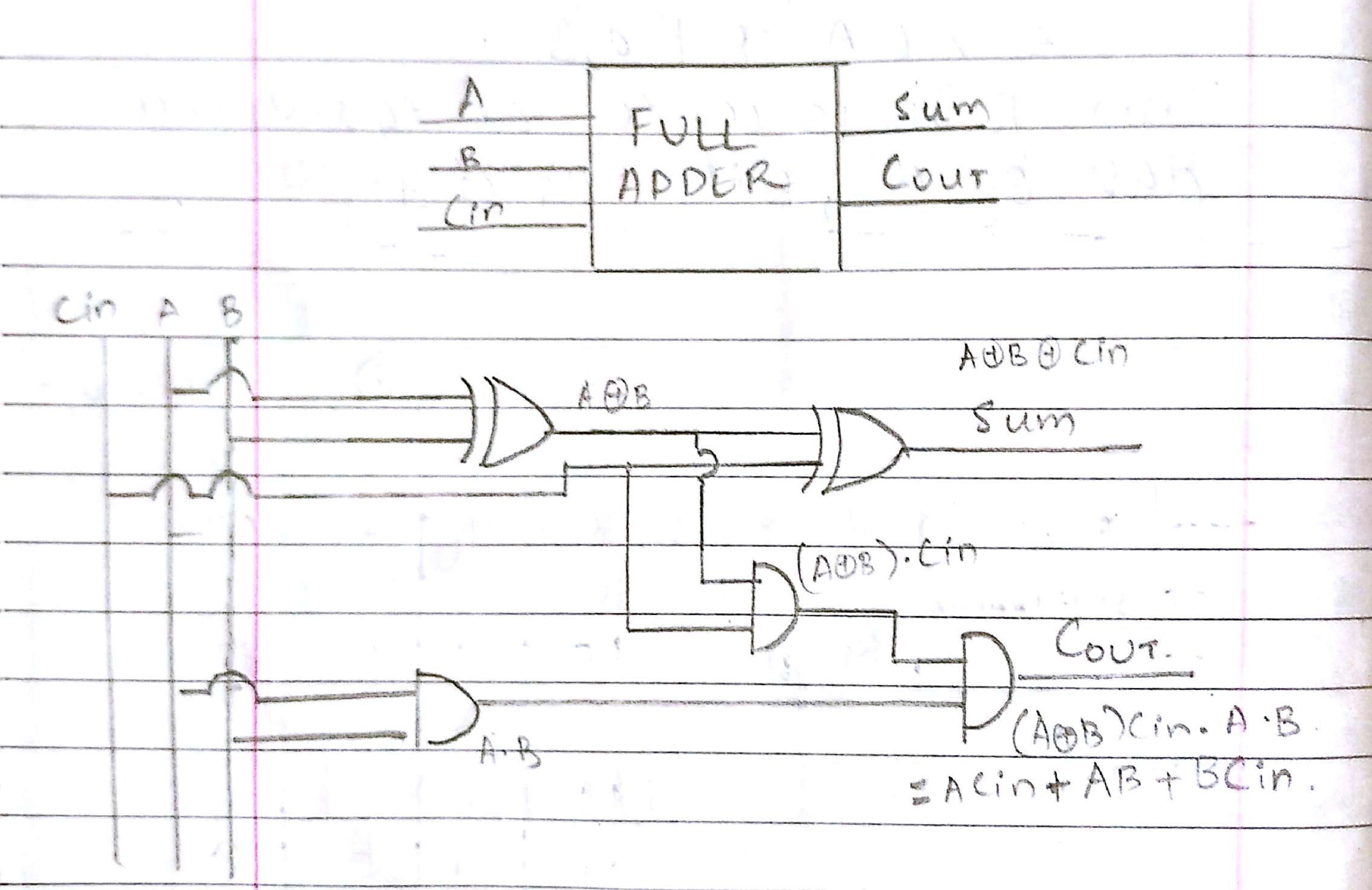


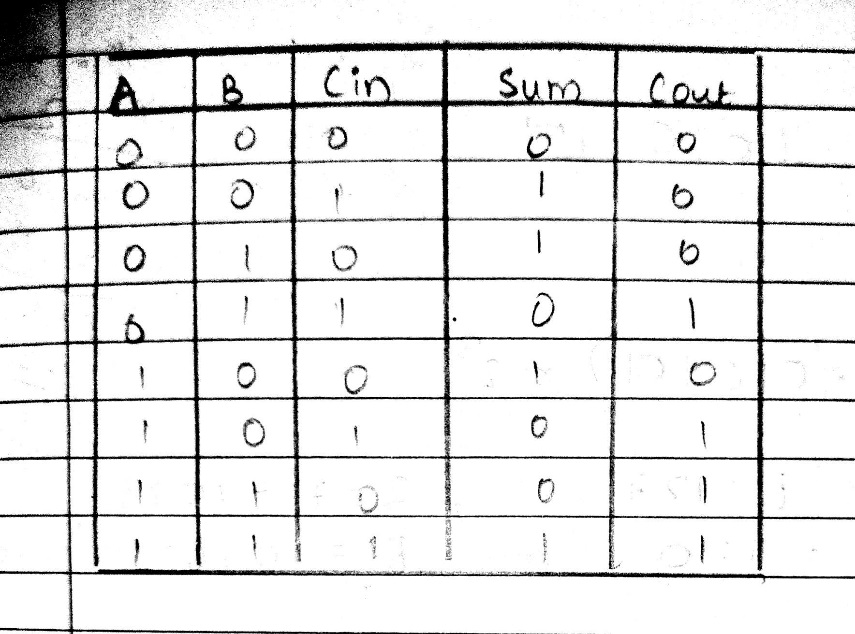
**From the truth table (with steps):**

S= AB’ +A’B

C=A.B

**Full Adder Block Diagram Truth Table for Full Adder**



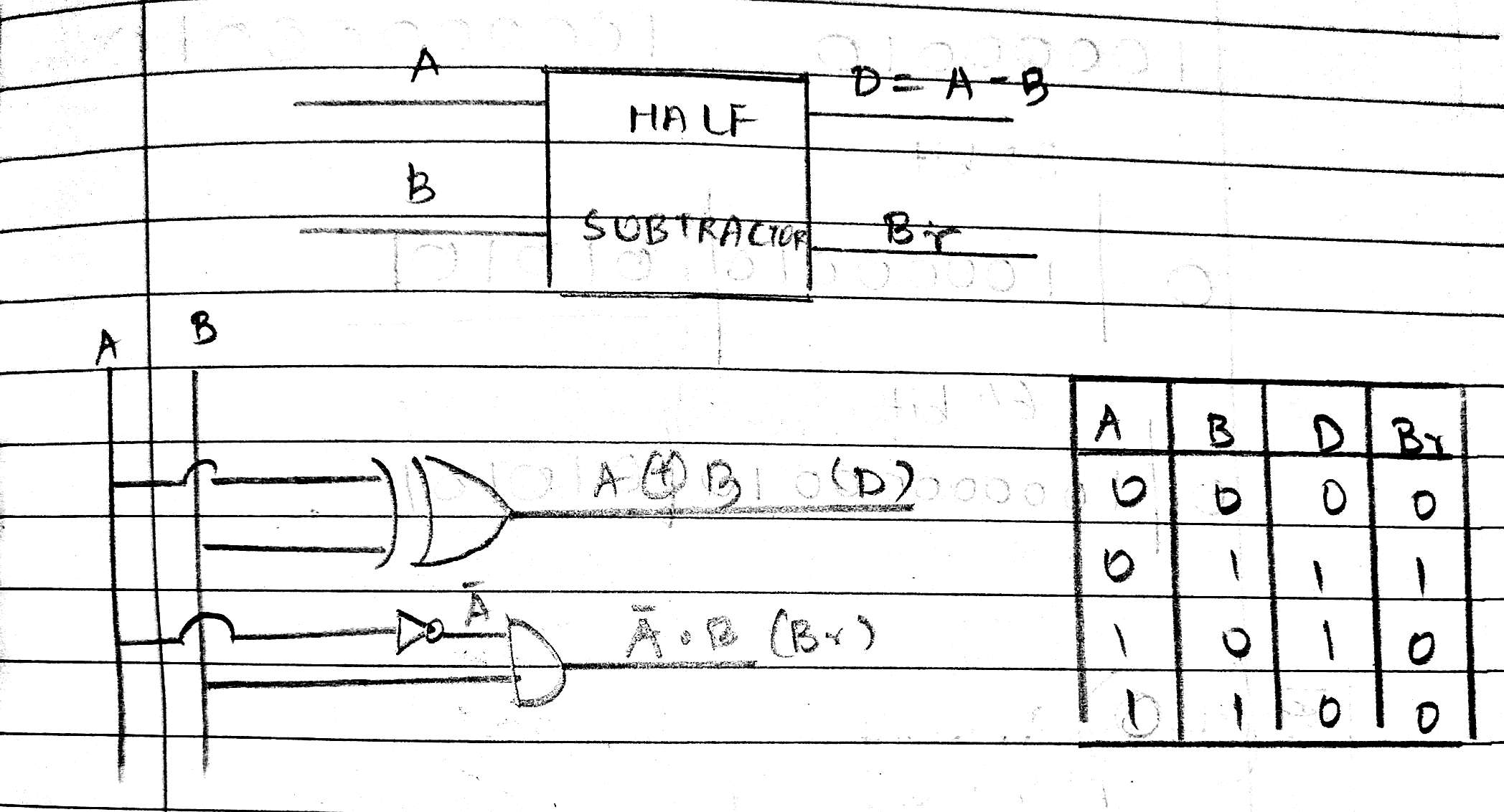


**From the truth table (with steps):**

S = A’B’Cin + A’BCin’ + AB’Cin’ + ABCin

Cout = ACin + AB+ BCin

**Half Subtractor Block Diagram Truth Table for Half Subtractor**

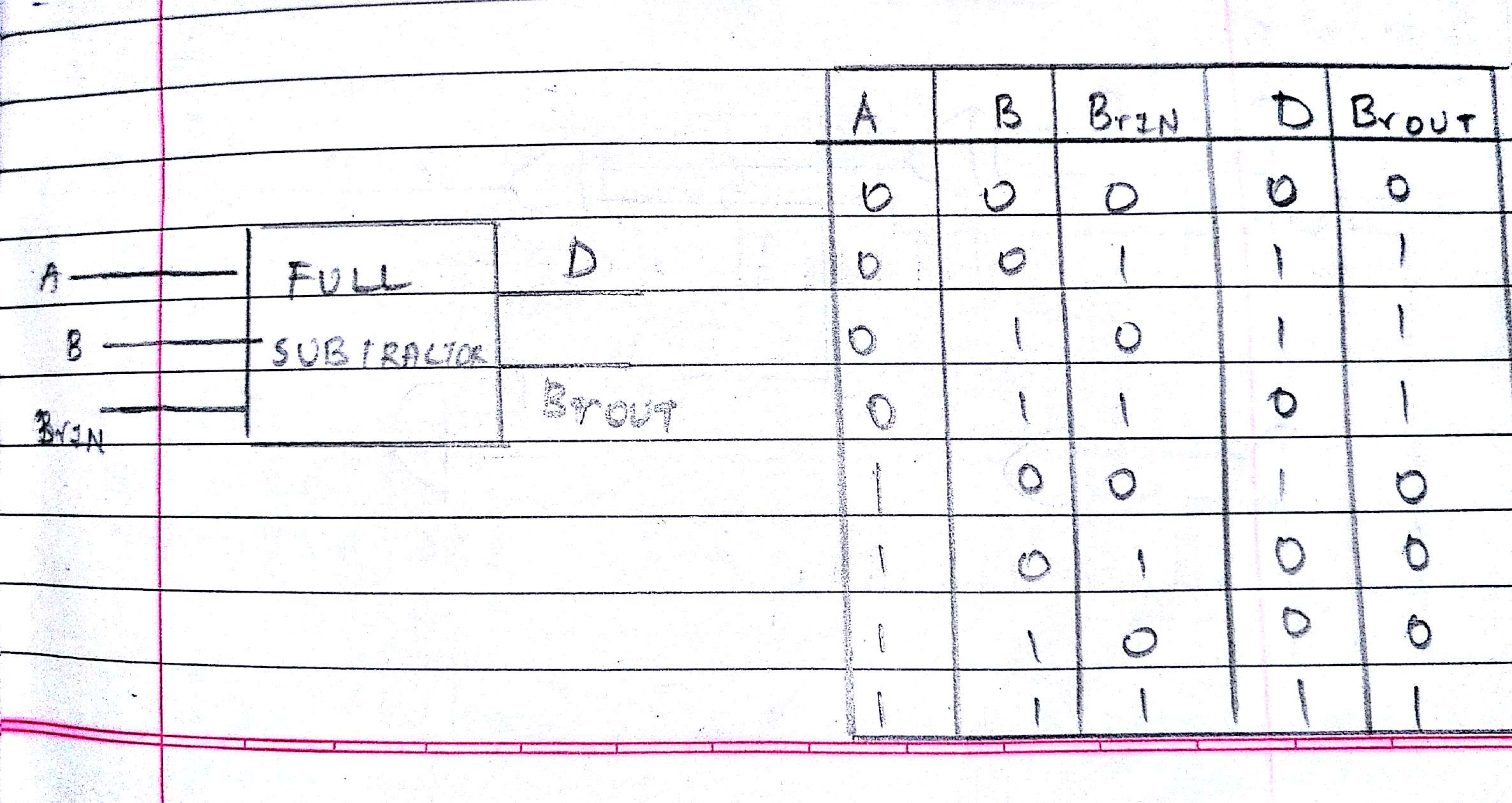


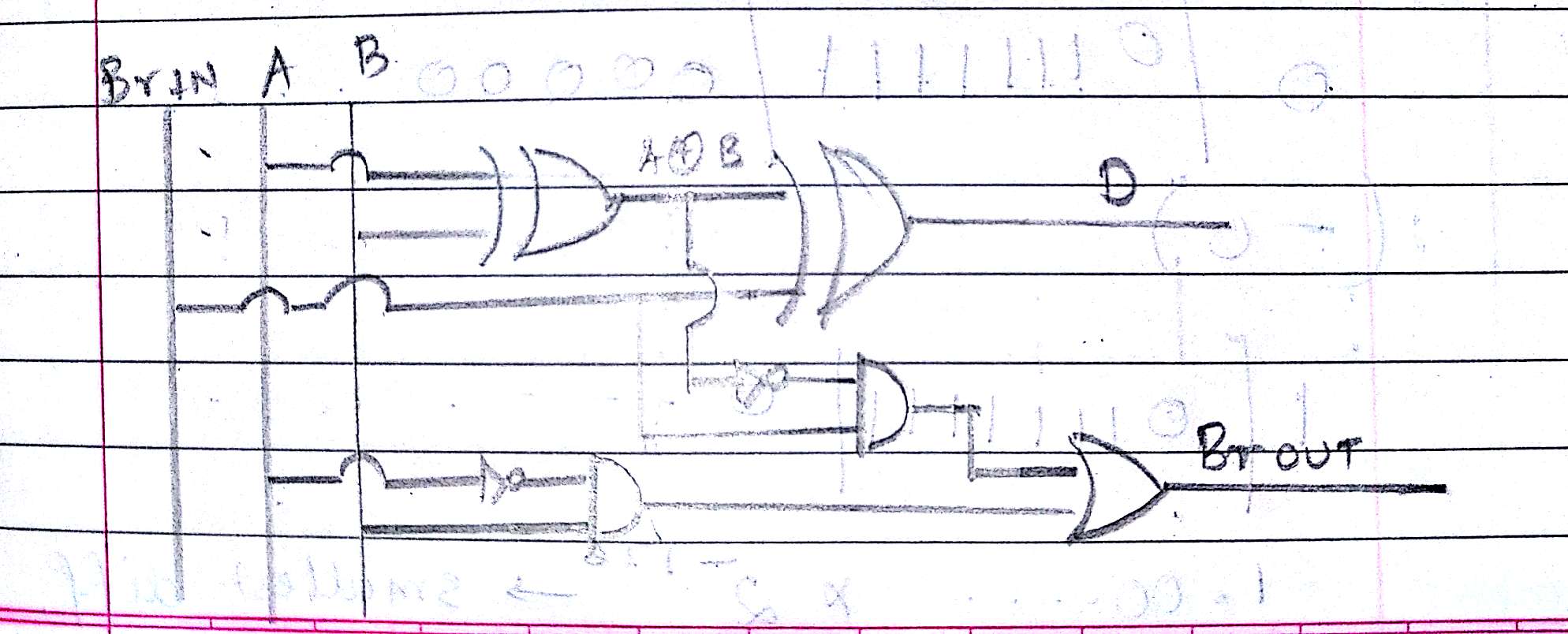
**From the truth table (with steps) :**

Difference (D) = A’B + AB’

Borrow(B) = A’B

**Full Subtractor Block Diagram Truth Table for Full subtractor**





**From the truth table (with steps):**

Differenc = A’B’Bin + A’BBin’ + AB’Bin’ + ABBin

Borrow out= A’B + A’Bin + BBin

**IC 7483**

**Procedure:**

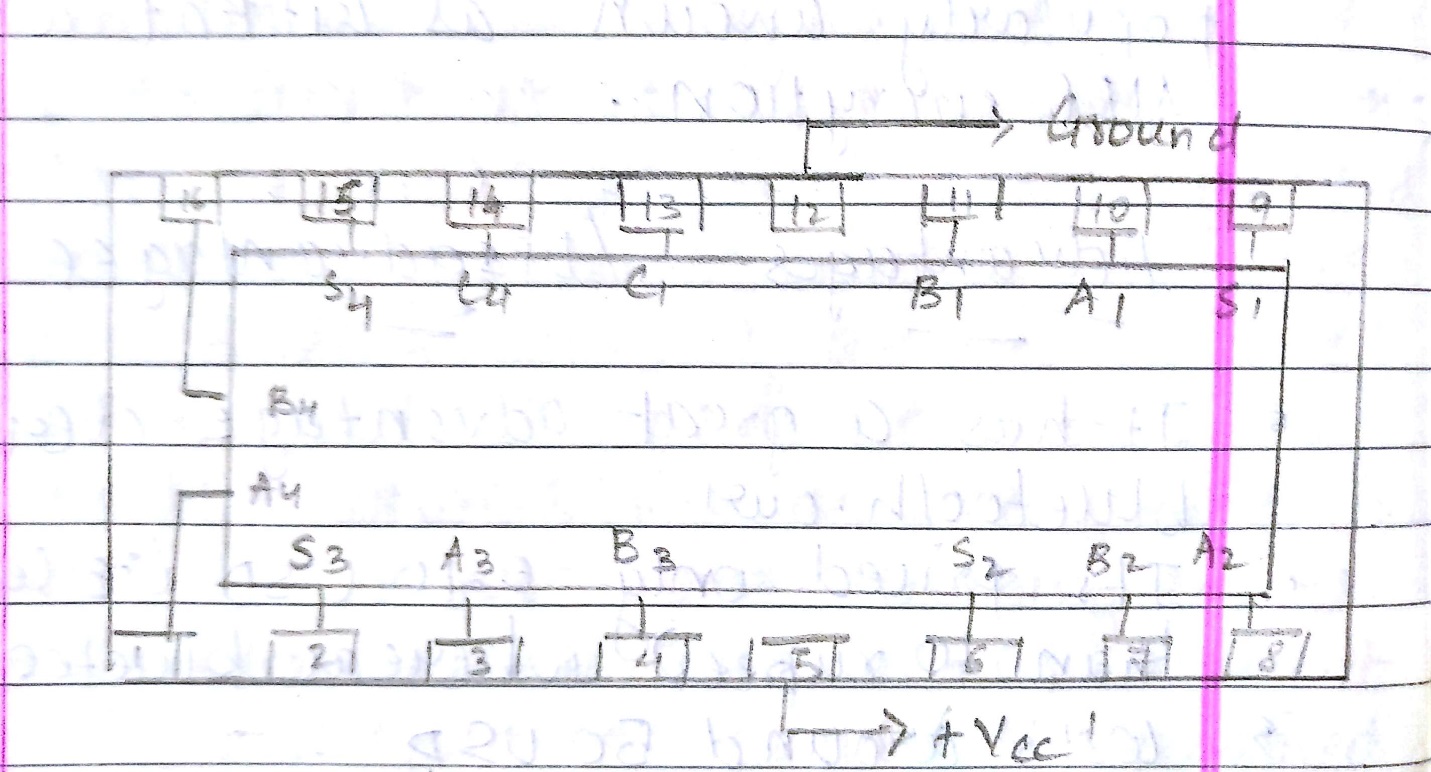
1. Locate the IC 7483 and 4-not gates block on trainer kit.
2. Connect 1st input no. to A4-A1 input slot and 2nd (negative) no. to B4-B1 through 4-not gates (1C of 2nd no.)
3. Connect high input to Co so that it will get added with 1C of 2nd no. to get 2C.
4. Connect 4-bit output to the output indicators.
5. Switch ON the power supply and monitor the output for various input combinations.

**Example:**

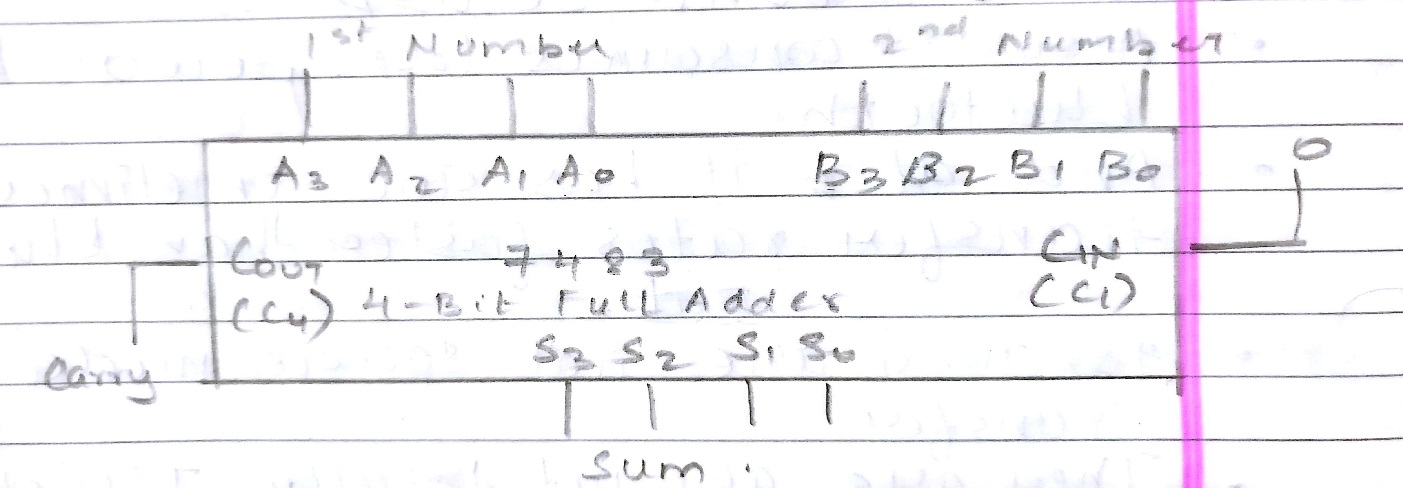
|  |  |  |
| --- | --- | --- |
| 1) 710 -210 = 510 | |  |
| 7 |  | 0111 |
| 2 |  | 0010 |
| 1’C of 2 | | 1101 |
|  |  | + 1 |
| 2’C of 2 | | 1110 |

0111 + 1110 1 0101

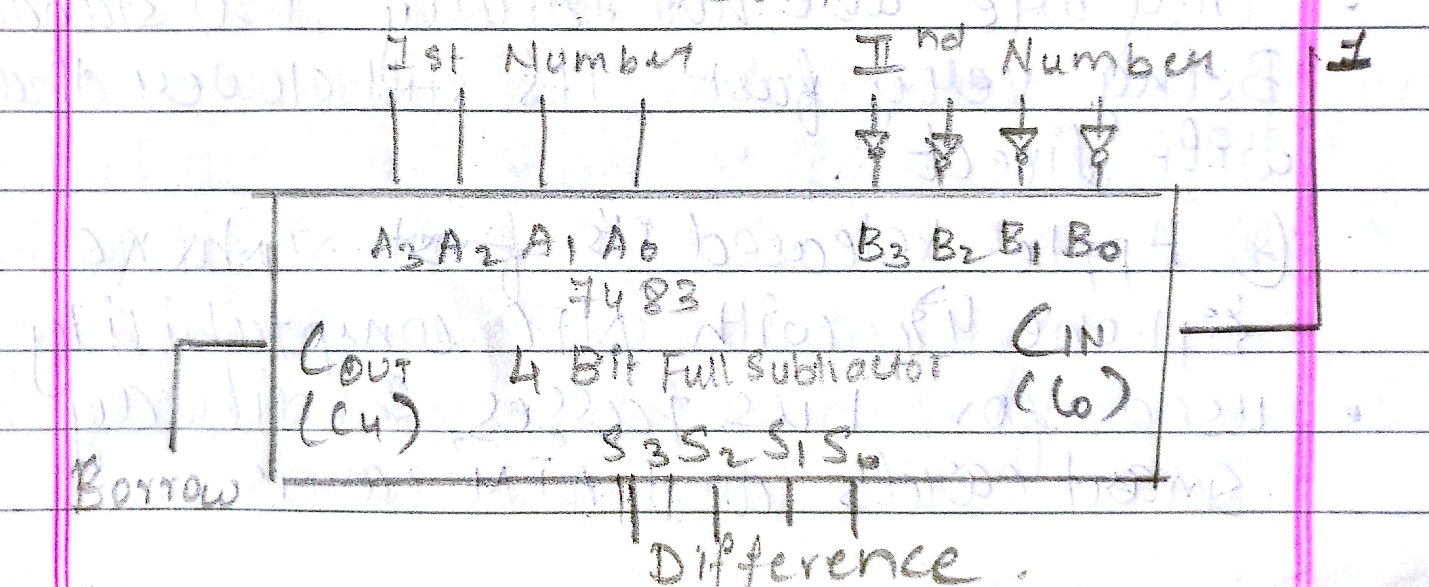
**Pin Diagram IC7483**

****

**Adder**

****

**Subtractor**

****

**Conclusion:**

Thus the circuit of binary adder and subtractor on the IC was successfully made and tested.

**Post Lab Descriptive Questions**

1. What is difference between half and full adder, half and full subtractor?

|  |  |
| --- | --- |
| Half Adder | Full Adder |
| 1. Half adder accepts two binary digits on it’s inputs and produce two binary digits outputs, a sum bit and a carry bit | The full adder accepts two input bits and an input carry and generates a sum output and an output carry |
| 1. Half adder is easier to implement. | It is more difficult as it needs two half adders to implement |
| 1. Half adder can add only two input bits (A and B) and has nothing to d owith carry if there is only one input, that means the binary addition process is not complete, thus it is called half adder. | Full adder can add a 3 bit number (A,B,Cin) A and B are the operands and Cin is the carry from the previous less significant stage. |

|  |  |
| --- | --- |
| Half Subtractor | Full Subtractor |
| It is a combinational circuit which is used to perform subtraction of two bits | It is a combinational circuit which is used to perform subtraction of three bits |
| It has two inputs (A,B) and two output D(Difference) and B(Borrow). | It has input A(number) B(subtractor) and Bin (Borrow) from previous stage. And the outputs are D (Difference) and B (Borrow) |
| Truth table :   |  |  |  |  | | --- | --- | --- | --- | | A | B | D | B | | 0 | 0 | 0 | 0 | | 0 | 1 | 1 | 1 | | 1 | 0 | 1 | 0 | | 1 | 1 | 0 | 0 | | Truth table:   |  |  |  |  |  | | --- | --- | --- | --- | --- | | A | B | Bin | A-B-Bin | Bout | | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 1 | 1 | 1 | | 0 | 1 | 0 | 1 | 1 | | 0 | 1 | 1 | 0 | 1 | | 1 | 0 | 0 | 1 | 0 | | 1 | 0 | 1 | 0 | 0 | | 1 | 1 | 0 | 0 | 0 | | 1 | 1 | 1 | 1 | 1 | |

1. Perform the following Binary subtraction with the help of appropriate ICs:
2. 7-5

Writing in binary form:

7= 111

5= 101

(7-5) = 111

-101

010

7-5 = (010)2

7-5= (2)10

1. 5-7

Writing in binary form:

7= 111

5= 101

1’s complement of 7 is 000

Adding 1 to 1’s complement = 000

+001

001

Adding 2’s complement of 7 to 5 we get

101

+001

110

Since the answer is negative,

Taking 2’s complement of the answer we get 001

+001

010

Thus, 5-7 = -2

1. 9 - 4

Writing in binary form:

9 = 1001

4 = 0100

Thus subtracting directly we get:

1001

-0100

0101

Therefore 9 - 4 = (0101)2

9 - 4 = 5